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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHEN, TE Y	

ART UNIT	PAPER NUMBER
2161	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,133	HAMMARLUND ET AL.	
	Examiner	Art Unit	
	Susan Y. Chen	2161	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11,13,18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11,13,18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

This office action is in response to the filed on May 02, 2005. Claims 2-11, 13, 18 and 20 are pending for examination, claims 1, 12 14-17 and 21-24 have been canceled and claims 2, 11 and 18 have been amended.

The previously allowable subject matters recited in the claims 9-10 are withdrawn because the instant amendment changed the scope of invention with every amended independent claims to control the claimed first and second components based on the first mask value, as such, the instant amendment initiated a new ground rejection as following.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2-8, 11,13 and 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ebrahim et al. (U.S. Patent No. 5,644,753).

As to claim 2, Ebrahim et al. (hereinafter referred as Ebrahim) discloses a system for sharing a resource between at least two components [e.g., col. 1, lines 8-16; Fig(s). 1 and 12 and associated texts], comprising:

a) a resource having a plurality of elements [e.g., the units: 108, 109, 120, 134, 140, etc. Fig. 1];

b) at least first and second components access the elements of the resource [e.g., the units 102-1 to 102-n, 108, etc. Fig. 1 and associated texts]

c) an access controller [e.g., the unit 110, Fig. 1] coupled to the resource and the at least first and second components [e.g., the units 102-1 to 102-n, Fig. 1] to stored a first mask value [e.g., The UPACAP field 161, Fig. 4 and associated texts], wherein access to the elements of the resource by the first and second components is controlled based on the first mask value [e.g., Fig. 4 and associated texts].

As to claim 3, except the features recited in claim 2, Ebrahim further discloses that the first mask value represents which of the elements of the resource are available for access for a selected component [col. 6, lines 23-39; col. 14, lines 39-57].

As to claim 4, Ebrahim discloses the features as claimed by applicant, comprising:

a) a memory resource having a plurality of addressable blocks [e.g., the units 108, 109, Fig. 1];

b) first and second components adapted to access the memory resource [e.g., the units: 104-1 to104-n, 120-1 to 120-n, 110, 112, 132, 134-1 to 134-n, etc, Fig(s). 1 and 12 and associated texts]; and

c) a register adapted to store a first mask value, wherein access to addressable blocks of the memory resource is controlled based on the first mask value [e.g., the unit 158, Fig. 4, the unit 180, Fig. 5 and 190, Fig. 6 and associated texts; col. 14, lines 16-57; col. 22, lines 5 – col. 23, line 40].

As to claim 5, except the features cited in claim 4, Ebrahim further discloses that the memory resource is a cache memory [e.g., Abstract, lines 1-5].

As to claim 6, except the features cited in claim 4, Ebrahim further discloses that a processor couple to the cache memory, wherein the first component includes execution of instructions by the processor from a first thread and the second component includes execution of instructions by the processor from a second thread [e.g., the unit 100, 102, Fig. 1 and associated texts; col. 6, lines 14-22; col. 17, lines 61 – col. 18, line 26; Fig(s). 5-7 and associated texts].

As to claim 7, except the features cited in claim 6, Ebrahim further discloses that the first mask value represent which of the addressable blocks of the cache memory are available for eviction [e, g., col. 1, lines 53-60; col. 20, lines 59 – col. 21, line 11].

As to claim 8, except the features cited in claim 7, Ebrahim further discloses that the first mask value is provided for each of the components to indicate which of the addressable blocks of the cache memory are available for eviction for at least two of the components [e.g., col. 1, lines 53-60; col. 20, lines 59 – col. 21, line 11; col. 31, lines 5 – 42].

As to claims 11, 13, 18 and 20, these claims recites the same subject matter as claims 2-8 in form of method and computer program product, hence are rejected for the same reason.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebrahim et al. (U.S. Patent No. 5,644,753) in view of Arimilli et al. (U.S. Patent No. 5,867,511).

As to claim 9, except the features cited in claim 7, Ebrahim further discloses an eviction array [e.g., the units: 132, 134, Fig. 1 and associated texts] and a second mask for selecting which bit of the eviction array are used I controlling which of the

addressable blocks of the cache memory are available for eviction [e.g., the unit 194, Fig. 6 and associated texts].

Ebrahim did not specifically disclose that the eviction array is indicating the least recently used addressable block of the cache memory.

However, Arimilli et al. (hereinafter referred as Arimilli) discloses [col. 2, lines 39-58; the units: 44, 46, etc Fig. 2 and associated texts].

Ebrahim and Arimilli are both in the same field to process cache memory via memory mask, therefore, with the teachings of Ebrahim and arimilli in front of him/her, it would have been obvious for an ordinary skilled person in the art at the time the invention was made being motivated to combine the well-known technique as taught by Arimilli into Ebrahim's system, because by doing so, as suggested by Arimilli the combined system will perform a must "evict" action when all of the blocks in a congruence class for a given cache are full, such that the combined system will free from memory crash. [e.g., col. 2, lines 39-58]

As to claim 10, this claim recites the same feature as claims 2-9 with different words, hence are rejected for the same reason.

Response to Arguments

Applicant's arguments filed on May 02, 2005 have been fully considered but they are not persuasive.

The examiner disagrees with applicant's arguments and misinterpretation that "Ebrahim fails to teach or suggest access to the element6s of the resource by the first and second component is controlled based on the first mask value, as claimed in claims 2, 11 and 18 as amended..."

In reply to these arguments, Applicant attention is directed to the recitation at col. 6,lines 11-39 and col. 14, lines 39-57, wherein, Ebrahim clearly disclosures the following:

"Referring to FIG. 1, there is shown a multiprocessor computer system 100 incorporating the computer architecture of the present invention. The multiprocessor computer system 100 includes a set of "UPA modules." UPA modules 102 include data processors as well as slave devices such as I/O handlers and the like. Each UPA module 102 has a port 104, herein called a UPA port, where "UPA" stands for "universal port architecture." For simplicity, UPA modules and their associated ports will often be called, collectively, "ports" or "UPA ports," with the understanding that the port or UPA port being discussed includes both a port and its associated UPA module."

"The system 100 further includes a main memory 108, which may be divided into multiple memory banks 109 $Bank_0$ to $Bank_m$, a system controller 110, and an interconnect module 112 for interconnecting the ports 104 and main memory 108. The interconnect module 112, under the control of datapath setup signals from the System Controller 110, can form a datapath between any port 104 and any other port 104 or between any port 104 and any memory bank 109. The interconnect module 112 can be as simple as a single, shared data bus with selectable access ports for each UPA port and memory module, or can be a somewhat more complex crossbar switch having m ports for m memory banks and n ports for n UPA ports, or can be a

combination of the two. The present invention is not dependent on the type of interconnect module 112 used, and thus the present invention can be used with many different interconnect module configurations." (col. 6, lines 11 -39)

"The UPACAP field 161 is a 5-bit mask field to indicate the capabilities of the UPA port. UPACAP[0] is set if UPA has a master interface. UPACAP[1] is set if the UPA module has a cache (making the UPA port a "CacheMaster"). UPACAP[2] is set if the UPA port has an interrupter interface using the UPA_SlaveInt_L signal. This bit is set primarily by slave-only UPA ports. Software assigns this UPA port a target-MID corresponding to an interrupt handler. UPACAP[3] is set if the UPA port has an interrupter interface using the P_INT_REQ transaction request protocol. Software assigns this UPA port a target-MID corresponding to an interrupt handler. UPACAP[4] is set if the UPA port has an interrupt handler interface. The System Controller forwards P_INT_REQ interrupt requests from other UPA ports to this port only if this bit is set." (col. 14, lines 39-57)

Thus, based on the above discussion, the claimed features clearly read by Ebrahim's disclosure as shown in Fig. 1 and the UPACAP 5-bit mask field (the unit: 161, Fig. 4).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Susan Y. Chen whose telephone number is 571-272-4016. The examiner can normally be reached on Monday - Friday from 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Safet Metjahic can be reached on 571-272-4023. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Susan Y Chen
Examiner
Art Unit 2161

July 1, 2005

UYEN LE
PRIMARY EXAMINER